

CLAIMS

1 1. (currently amended) Circuitry comprising a first differential transistor pair (e.g., M₆,
2 M₇) connected between a first load device (e.g., M₄) and a first current sink (e.g., 102), wherein:

3 a first inductance-creating element (e.g., M₂) is connected to the first load device to add
4 inductance at a first output node (e.g., V_{ON}) of the circuitry; and

5 a power-supply rejection element (e.g., M₁ and H) is connected between the first inductance-
6 creating element and a first voltage reference (e.g., V_{DD}) to provide power-supply rejection at the first
7 output node.

1 2. (currently amended) The invention of claim 1, further comprising:

2 a second load device (e.g., M₅) connected to the first differential transistor pair; and

3 a second inductance-creating element (e.g., M₃) connected to the second load device to add
4 inductance at a second output node (e.g., V_{OP}) of the circuitry, wherein the power-supply rejection
5 element is connected between the second inductance-creating element and the first voltage reference to
6 provide power-supply rejection at the second output node.

1 3. (currently amended) The invention of claim 2, further comprising a second differential
2 transistor pair (e.g., M₈, M₉ of Fig. 2) connected between the first and second load devices and a second
3 current sink (e.g., 104) such that the circuitry is adapted to provide a variable-gain amplifier (VGA)
4 function.

1 4. (original) The invention of claim 3, wherein, when current through the first current sink
2 increases, current through the second current sink is adapted to decrease such that total current through
3 the first and second current sinks remains substantially constant to provide the VGA function with near
4 exponential gain control.

1 5. (currently amended) The invention of claim 3, further comprising:

2 a common-mode sense circuit (e.g., 206) connected to the first and second output nodes and
3 adapted to generate a sensed common-mode voltage signal (e.g., 208); and

4 a differential amplifier (e.g., 207) connected to receive the sensed common-mode voltage signal
5 and a desired common mode voltage signal (e.g., V_{cmref}) and adapted to generate and apply a common-
6 mode error-correction signal to the first and second inductance-creating elements to correct for
7 differences between the sensed and the desired common-mode voltage signals.

1 6. (currently amended) The invention of claim 5, further comprising:

2 a first capacitor (e.g., CL₁ of Fig. 3) connected between the first output node and a second
3 reference voltage (e.g., V_{SS}); and

4 a second capacitor (e.g., CL₂) connected between the second output node and the second
5 reference voltage such that the circuitry is adapted to provide a continuous-time filter (CTF) function in
6 addition to the VGA function.

1 7. (original) The invention of claim 6, wherein the first and second capacitors are variable
2 capacitors.

1 8. (currently amended) The invention of claim 6, wherein the power-supply rejection
2 element comprises a current source (e.g., H) whose current is controlled by a control signal that is
3 adapted to be adjusted to adjust equivalent resistance provided by the first and second inductance-
4 creating elements.

1 9. (currently amended) The invention of claim 2, further comprising:
2 a common-mode sense circuit (e.g., ~~206~~) connected to the first and second output nodes and
3 adapted to generate a sensed common-mode voltage signal (e.g., ~~208~~); and
4 a differential amplifier (e.g., ~~207~~) connected to receive the sensed common-mode voltage signal
5 and a desired common mode voltage signal (e.g., V_{CMREF}) and adapted to generate and apply a common-
6 mode error-correction signal to the first and second inductance-creating elements to correct for
7 differences between the sensed and the desired common-mode voltage signals.

1 10. (currently amended) The invention of claim 9, further comprising:
2 a first capacitor (e.g., ~~CL1~~ of Fig. 4) connected between the first output node and a second
3 reference voltage; and
4 a second capacitor (e.g., ~~CL2~~) connected between the second output node and the second
5 reference voltage such that the circuitry is adapted to provide a continuous-time filter (CTF) function.

1 11. (original) The invention of claim 10, wherein the first and second capacitors are variable
2 capacitors.

1 12. (currently amended) The invention of claim 10, wherein the power-supply rejection
2 element comprises a current source (e.g., ~~I1~~) whose current is controlled by a control signal that is
3 adapted to be adjusted to adjust equivalent resistance provided by the first and second inductance-
4 creating elements.

1 13. (currently amended) The invention of claim 1, further comprising:
2 a second load device (e.g., ~~M5~~ of Fig. 2) connected to the first differential transistor pair;
3 a second inductance-creating element (e.g., ~~M3~~) connected to the second load device to add
4 inductance at a second output node (e.g., V_{OP}) of the circuitry, wherein the power-supply rejection
5 element is connected between the second inductance-creating element and the first voltage reference to
6 provide power-supply rejection at the second output node;
7 a second differential transistor pair (e.g., ~~M8, M9~~) connected between the first and second load
8 devices and a second current sink (e.g., ~~104~~) such that the circuitry is adapted to provide a variable-gain
9 amplifier (VGA) function;
10 a common-mode sense circuit (e.g., ~~206~~) connected to the first and second output nodes and
11 adapted to generate a sensed common-mode voltage signal (e.g., ~~208~~); and
12 a differential amplifier (e.g., ~~207~~) connected to receive the sensed common-mode voltage signal
13 and a desired common mode voltage signal (e.g., V_{CMREF}) and adapted to generate and apply a common-
14 mode error-correction signal to the first and second inductance-creating elements to correct for
15 differences between the sensed and the desired common-mode voltage signals, wherein:
16 the first differential transistor pair comprises transistor M6 and transistor M7;
17 the second differential transistor pair comprises transistor M8 and transistor M9;
18 the first load device comprises transistor M4;
19 the second load device comprises transistor M5;
20 the first inductance-creating element comprises transistor M2;
21 the second inductance-creating element comprises transistor M3;
22 the power-supply rejection element comprises transistor M1 and current source I1;
23 a first input node V_{IN} is connected to the gates of transistors M6 and M9;
24 a second input node V_{IN} is connected to the gates of transistors M7 and M8;
25 the sources of transistors M6 and M7 are connected to the first current sink;
26 the sources of transistors M8 and M9 are connected to the second current sink;
27 the drains of transistors M6 and M8 are connected to the first output node V_{ON} and to the source
28 of transistor M4;

29 the drains of transistors M7 and M9 are connected to the second output node V_{ON} and to the
30 source of transistor M5;

31 the drains of transistors M4 and M5 are connected to the first reference voltage V_{DD} ;
32 the gate of transistor M4 is connected to the drain of transistor M2;
33 the gate of transistor M5 is connected to the drain of transistor M3;
34 the sources of transistors M1, M2, and M3 are connected together and to receive the common-
35 mode error-correction signal; and
36 the gates of transistors M1, M2, and M3 and the drain of transistor M1 are connected together
37 and to receive the current from current source I1.

1 14. (original) The invention of claim 13, wherein, when current through the first current
2 sink increases, current through the second current sink is adapted to decrease such that total current
3 through the first and second current sinks remains substantially constant to provide the VGA function
4 with near exponential gain control.

1 15. (currently amended) The invention of claim 13, further comprising:
2 a first variable capacitor (e.g., CL1 of Fig. 3) connected between the first output node and a
3 second reference voltage; and
4 a second variable capacitor (e.g., CL2) connected between the second output node and the
5 second reference voltage such that the circuitry is adapted to provide a continuous-time filter (CTF)
6 function in addition to the VGA function.

1 16. (original) The invention of claim 15, wherein the current of current source I1 is
2 controlled by a control signal that is adapted to be adjusted to adjust equivalent resistance provided by
3 transistors M2 and M3.

1 17. (currently amended) The invention of claim 1, further comprising:
2 a second load device (e.g., M5 of Fig. 4) connected to the first differential transistor pair;
3 a second inductance-creating element (e.g., M3) connected to the second load device to add
4 inductance at a second output node (e.g., V_{OP}) of the circuitry, wherein the power-supply rejection
5 element is connected between the second inductance-creating element and the first voltage reference to
6 provide power-supply rejection at the second output node;
7 a common-mode sense circuit (e.g., 206) connected to the first and second output nodes and
8 adapted to generate a sensed common-mode voltage signal (e.g., 208);
9 a differential amplifier (e.g., 207) connected to receive the sensed common-mode voltage signal
10 and a desired common mode voltage signal (e.g., V_{CMREF}) and adapted to generate and apply a common-
11 mode error-correction signal to the first and second inductance-creating elements to correct for
12 differences between the sensed and the desired common-mode voltage signals;
13 a first variable capacitor (e.g., CL1) connected between the first output node and a second
14 reference voltage; and
15 a second variable capacitor (e.g., CL2) connected between the second output node and the
16 second reference voltage such that the circuitry is adapted to provide a continuous-time filter (CTF)
17 function, wherein:
18 the first differential transistor pair comprises transistor M6 and transistor M7;
19 the first load device comprises transistor M4;
20 the second load device comprises transistor M5;
21 the first inductance-creating element comprises transistor M2;
22 the second inductance-creating element comprises transistor M3;
23 the power-supply rejection element comprises transistor M1 and current source I1;
24 a first input node VIP is connected to the gates of transistors M6 and M9;

25 a second input node V_{IN} is connected to the gates of transistors M7 and M8;
26 the sources of transistors M6 and M7 are connected to the first current sink;
27 the drain of transistor M6 is connected to the first output node V_{ON} and to the source of
28 transistor M4;
29 the drain of transistor M7 is connected to the second output node V_{ON} and to the source of
30 transistor M5;
31 the drains of transistors M4 and M5 are connected to the first reference voltage V_{DD} ;
32 the gate of transistor M4 is connected to the drain of transistor M2;
33 the gate of transistor M5 is connected to the drain of transistor M3;
34 the sources of transistors M1, M2, and M3 are connected together and to receive the common-
35 mode error-correction signal; and
36 the gates of transistors M1, M2, and M3 and the drain of transistor M1 are connected together
37 and to receive the current from current source I1.

1 18. (original) The invention of claim 17, wherein the current of current source I1 is
2 controlled by a control signal that is adapted to be adjusted to adjust equivalent resistance provided by
3 transistors M2 and M3.